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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,880	12/19/2001	John Guzek	42390P13271	1290

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,880	GUZEK ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims **16 – 20** have been cancelled in Applicant's Response filed on September 2, 2003.

2. Claims **1 – 15** are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim**1** is rejected under 35 U.S.C. 102(b) as being anticipated by Gandhi et al. (US Patent No. 6,085,415).

Regarding claim 1, figures 7 – 17 illustrate a metal substrate 10 for electronics packaging (abstract, col. 6, lines 32 – 36) including a first region, and a second region electrically isolated from the first region by insolating 25 and 26 (claim 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **2 – 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gandhi et al. (US Patent No. 6,085,415) in view of Ahn et al. (US Patent No. 6,432,724).

Regarding claims **2 – 7**, Gandhi et al. disclose the claimed invention of claim 1 and the metal substrate core taught by Gandhi et al. is inherently included power or ground planes (col. 3, lines 35 – 43) but fail to explicitly teach at least one of the regions of the substrate core is coupled with digital ground of an integrated circuit; illustrate at least one of the regions of the substrate core is coupled with analog ground of an integrated circuit chip.

It is conventional and also taught by Ahn et al. that multiple chips mounted on the single substrate in a system module typically include different circuits, i.e., some analog circuits and some digital circuits. This requires a low impedance ground 106 (fig. 7) in the system module to suppress digital noise that may appear in the analog circuits of these mixed mode circuits (col. 1, lines 36 – 41)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form metal substrate core in Gandhi et al.'s integrated circuit chip package with a buried low impedance ground as taught by Ahn et al. in order to suppress digital noise in the analog circuits of a single substrate.

Regarding claims **8 – 11**, figures 7 – 17 illustrate a metal substrate 10 for electronics packaging (abstract, col. 6, lines 32 – 36) including a first region, and a second region electrically isolated from the first region by insolating 25 and 26 (claim 1). It is notice that the metal substrate core taught by Gandhi et al. is inherently included power or ground planes

(col. 3, lines 35 – 43). Gandhi et al. do not explicitly teach at least one of the regions of the substrate core is coupled with digital ground of an integrated circuit; illustrate at least one of the regions of the substrate core is coupled with analog ground of an integrated circuit chip. However, it is conventional and also taught by Ahn et al. that multiple chips mounted on the single substrate in a system module typically include different circuits, i.e., some analog circuits and some digital circuits. This requires a low impedance ground 106 (fig. 7) in the system module to suppress digital noise that may appear in the analog circuits of these mixed mode circuits (col. 1, lines 36 – 41)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form metal substrate core in Gandhi et al.'s integrated circuit chip package with a buried low impedance ground as taught by Ahn et al. in order to suppress digital noise in the analog circuits of a single substrate.

Regarding claims **12 – 15**, figures 7 – 17 illustrate a metal substrate 10 for electronics packaging (abstract, col. 6, lines 32 – 36) including a first region, and a second region electrically isolated from the first region by insolating 25 and 26 (claim 1). It is notice that the metal substrate core taught by Gandhi et al. is inherently included power or ground planes (col. 3, lines 35 – 43). Gandhi et al. do not explicitly teach at least one of the regions of the substrate core is coupled with digital ground of an integrated circuit; illustrate at least one of the regions of the substrate core is coupled with analog ground of an integrated circuit chip.

It is conventional and also taught by Ahn et al. that multiple chips mounted on the single substrate in a system module typically include different circuits, i.e., some analog

circuits and some digital circuits. This requires a low impedance ground 106 (fig. 7) in the system module to suppress digital noise that may appear in the analog circuits of these mixed mode circuits (col. 1, lines 36 – 41)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form metal substrate core in Gandhi et al.'s integrated circuit chip package with a buried low impedance ground as taught by Ahn et al. in order to suppress digital noise in the analog circuits of a single substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 703-305-5482. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Long Tran

October 17, 2003

HOAI HO
PRIMARY EXAMINER